

Figure 1: Pipeline CDS Circuit (Prior Art)

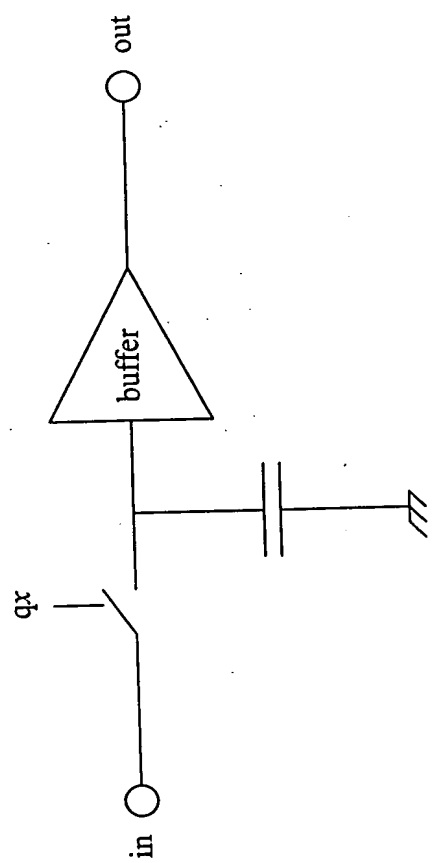
[illegible]

Figure 2: Sample-and-Hold (S/H) Circuit (Prior Art)



Figure 3: Dual CDS Circuit (Prior Art)

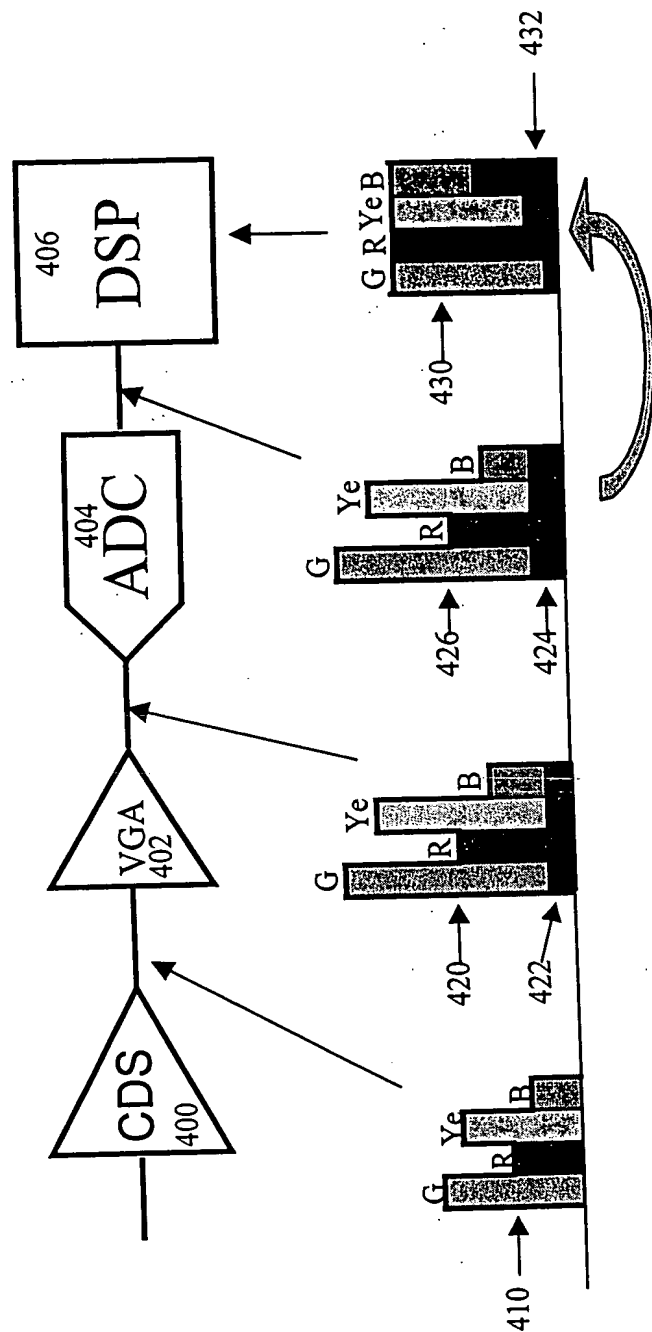


Figure 4: CCD Signal Processing Channel (Prior Art)

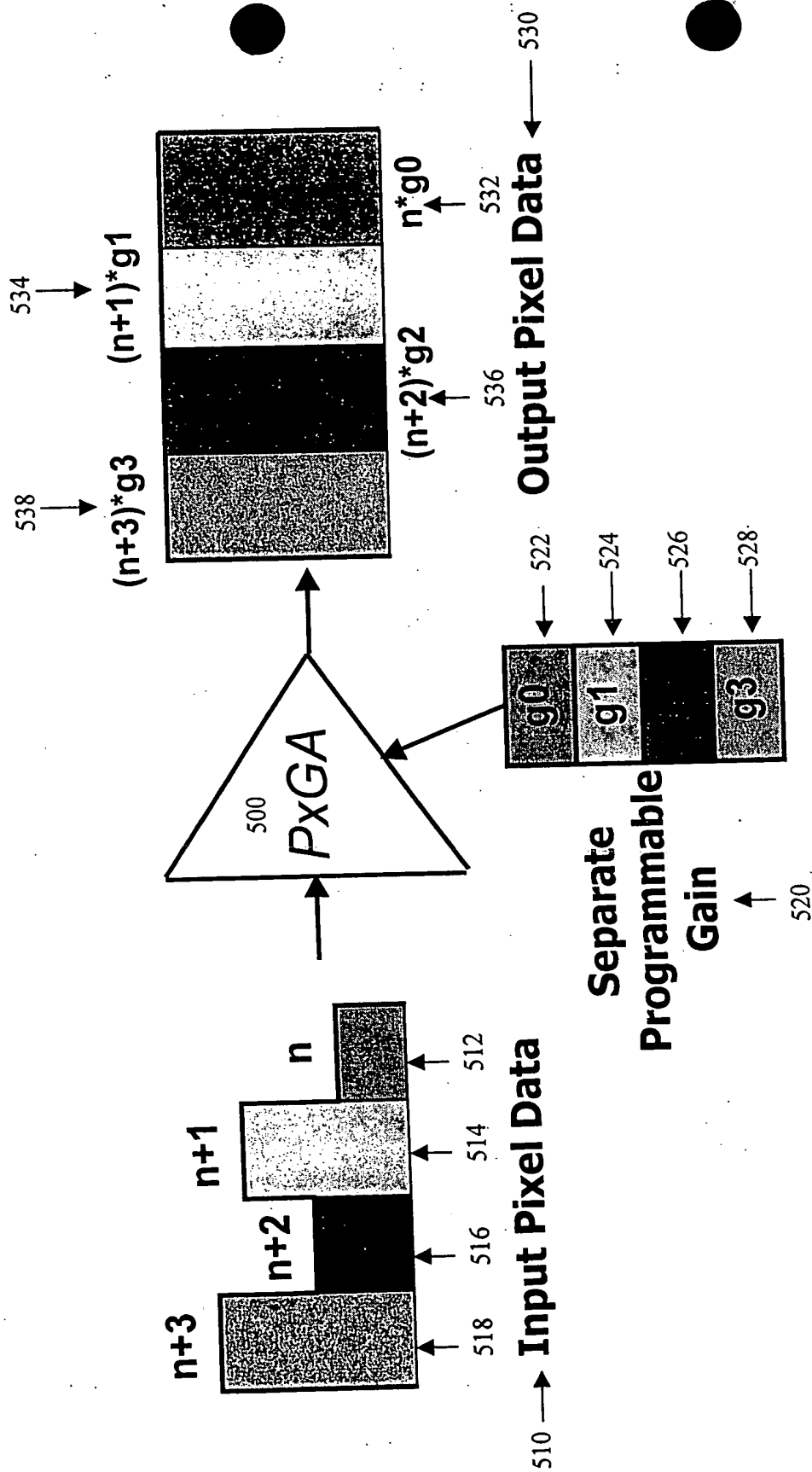


Figure 5: Pixel Gain Amplifier (PxGA)

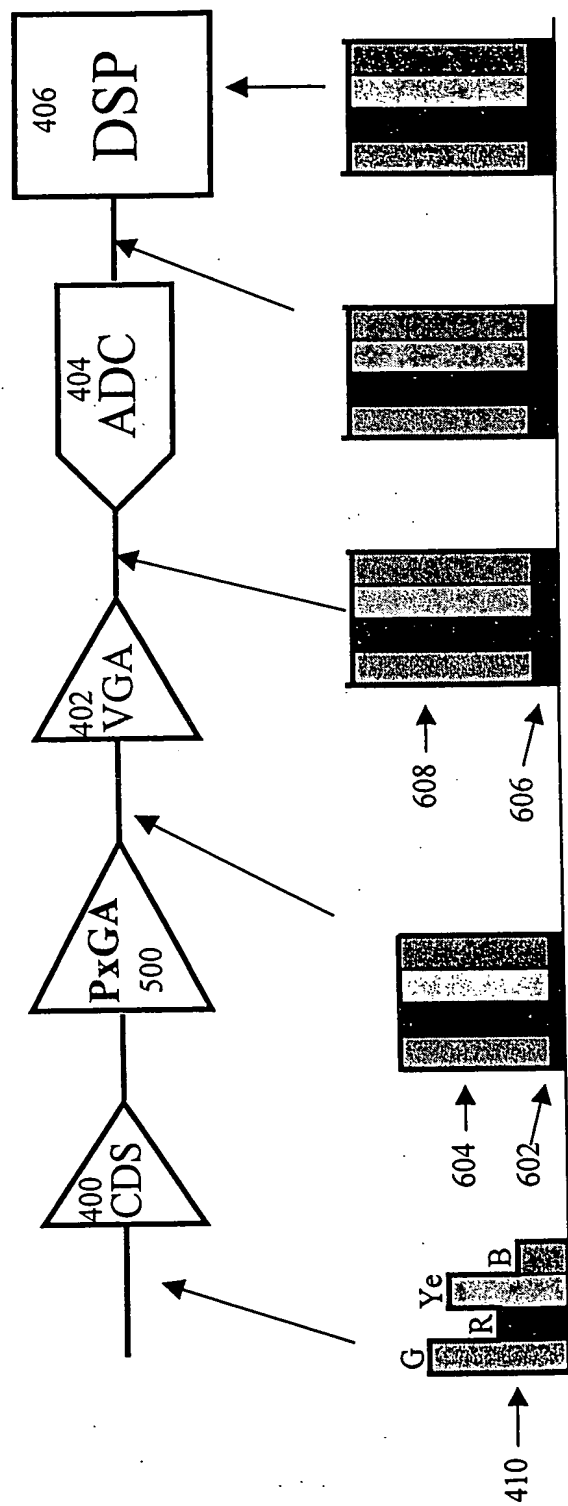


Figure 6: CCD Signal Processing Channel with PxGA

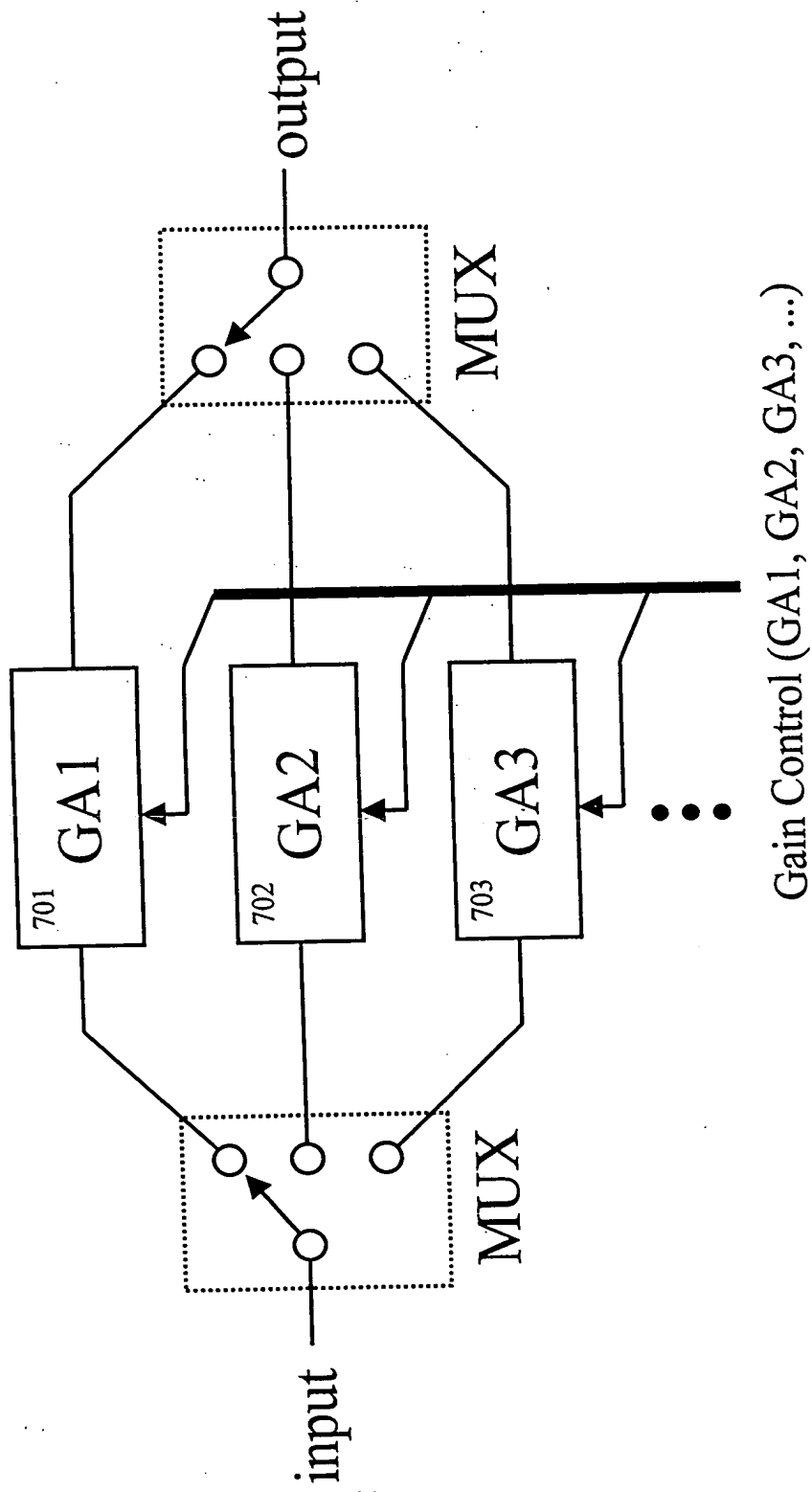


Figure 7: Multiplexed Gain Amplifier (Prior Art)

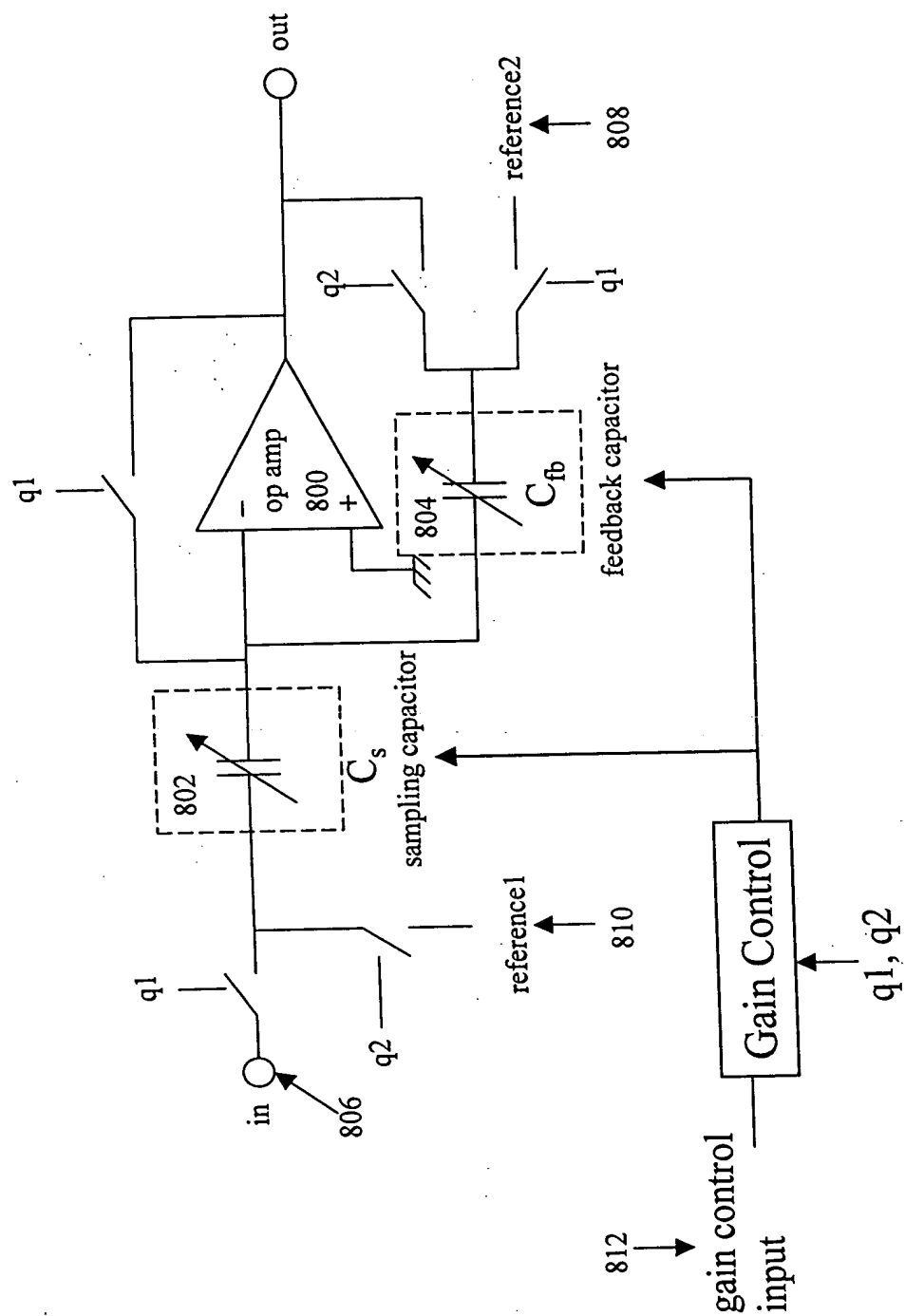


Figure 8(a): PxGA schematic



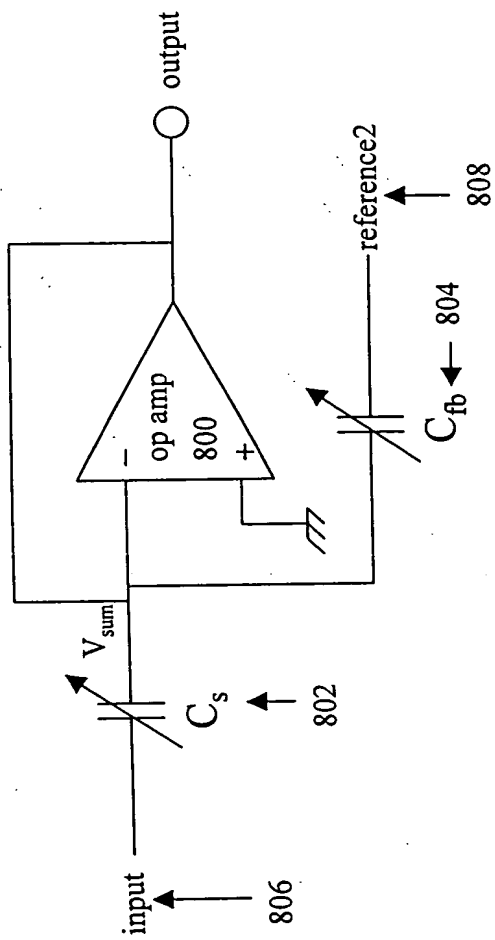


Figure 8(b): PxGA in q1 phase

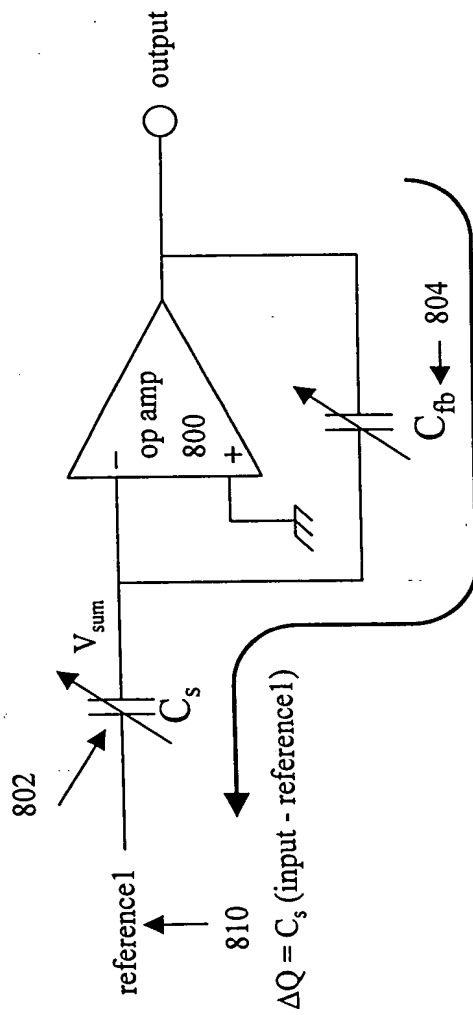


Figure 8(c): PxGA in q2 phase

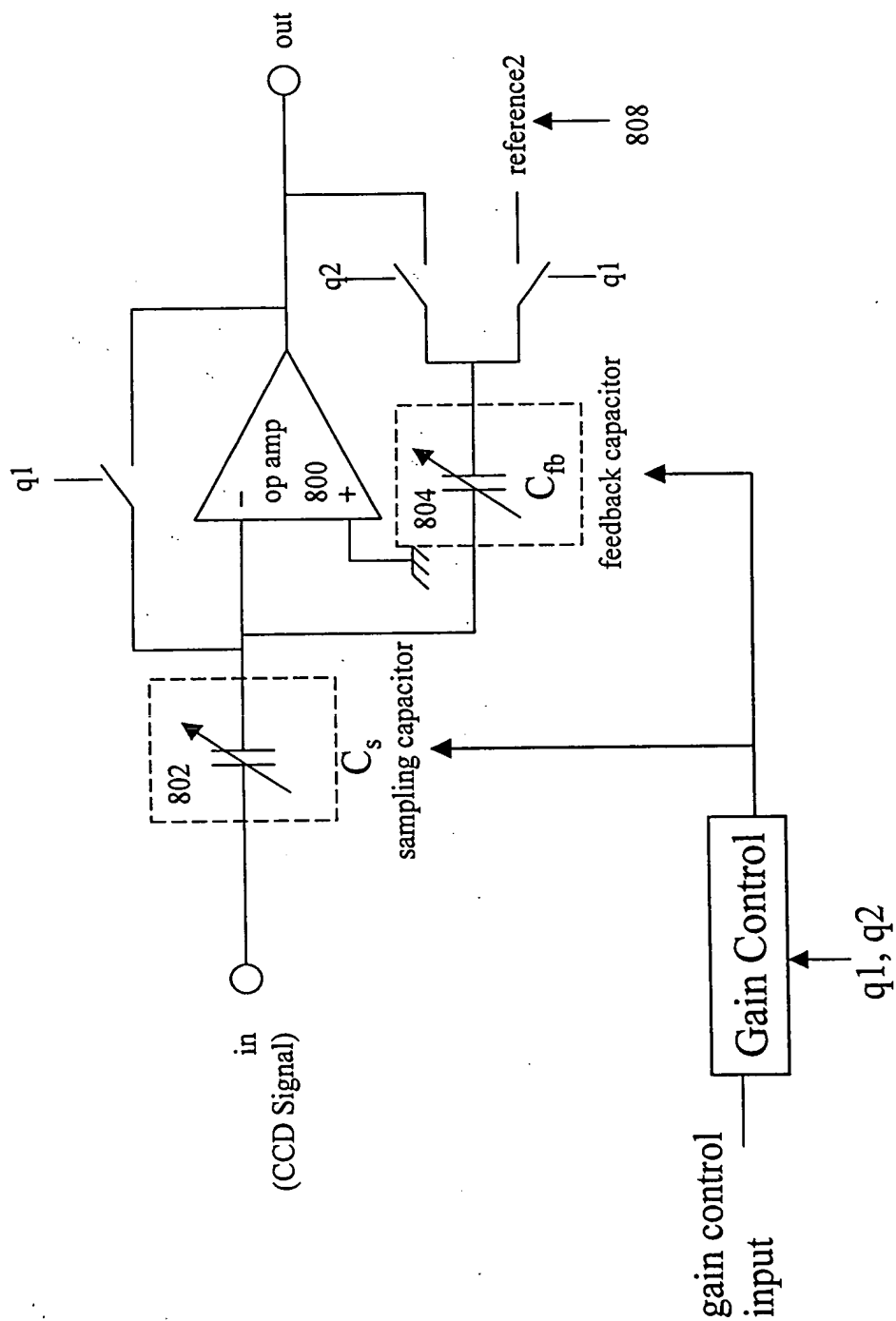


Figure 9: CDS/PxGA schematic



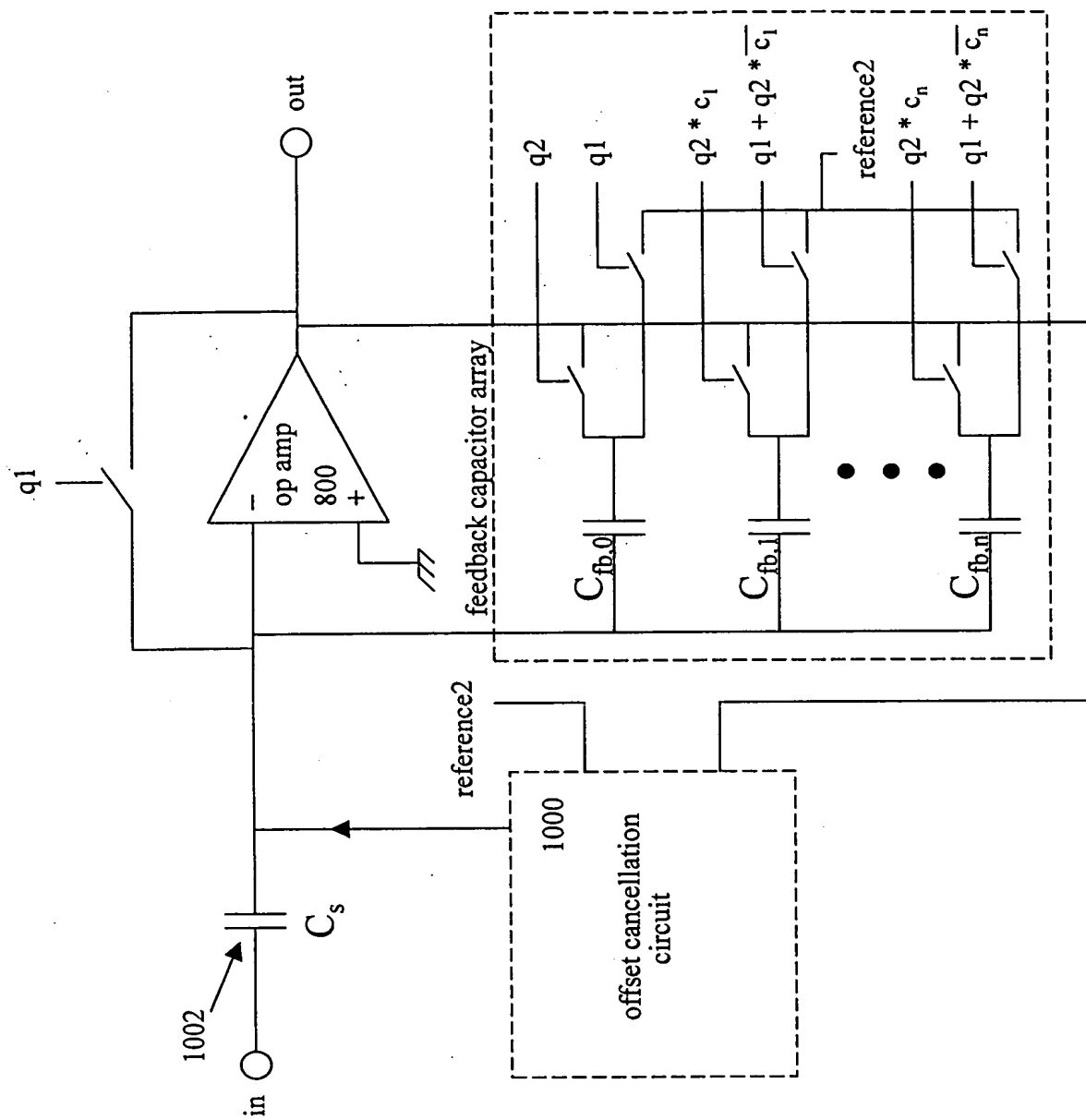


Figure 11: Implementation of Feedback Capacitor Array